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PATENT
Customer No. 22,852
Attorney Docket No. 6720.0070-00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
Ming-Dou KER et al.) Group Art Unit: 2811
Application No.: 10/062,714) Examiner: NOT YET ASSIGNED
Filed: February 5, 2002)
For: SCR DEVICES IN SILICON-ON-)
INSULATOR CMOS PROCESS FOR)
ON-CHIP ESD PROTECTION)

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicants bring to the attention of the Examiner the documents listed on the attached PTO 1449. This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits for the above-referenced application.

Copies of the listed documents, including any copending patent applications, are attached.

Applicants respectfully request that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed

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documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicants determine that the cited documents do not constitute "prior art" under United States law, applicants reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents.


Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

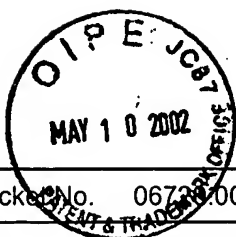
FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: May 10, 2002

By: 
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INFORMATION DISCLOSURE CITATION

Atty. Docket No.	067300070-00	Serial No.	10/062,714
Applicant Ming-Dou KER, et al.			
Filing Date	February 5, 2002	Group:	2811

U.S. PATENT DOCUMENTS

Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
VAMJ	5,910,874	06/08/1999	Iniewski et al.			
VAMJ	5,646,808	07/08/1997	Nakayama			
VAMJ	5,519,242	05/21/1996	Avery			
VAMJ	5,631,793	05/20/1997	Ker et al.			
VAMJ	5,811,857	09/22/1998	Assaderaghi et al.			
VAMJ	5,502,328	03/26/96	Chen et al.			
VAMJ	5,581,104	12/03/96	Lowrey et al.			
VAMJ	5,990,520	11/23/99	Noorlag et al.			

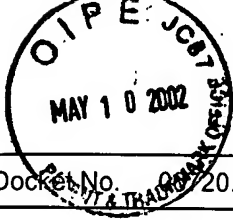
FOREIGN PATENT DOCUMENTS

Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

VAMJ	M-D. KER, et al., "CMOS On-Chip ESD Protection Design with Substrate-triggering Technique," Proc. of ICECS, Vol. 1, pp. 273-276, 1998
VAMJ	C. Duvvury et al., "Dynamic Gate Coupling for NMOS for Efficient Output ESD Protection", Proc. of IRPS, pp. 141-150, 1992

Examiner	<i>Victor A. Mandalaga</i>	Date Considered	12-13-02
*Examiner:	Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		
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INFORMATION DISCLOSURE CITATION

Atty. Docket No.	20.0070-00	Serial No.	10/062,714
Applicant	Ming-Dou KER, et al.		
Filing Date	February 5, 2002	Group:	2811

U.S. PATENT DOCUMENTS

Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
VAMJ	5,907,462	05/25/99	Chatterjee et al.			
VAMJ	5,932,918	08/03/99	Krakauer			
VAMJ	6,015,992	01/18/00	Chatterjee et al.			
VAMJ	5,453,384	09/26/95	Chatterjee			

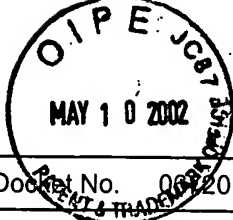
FOREIGN PATENT DOCUMENTS

Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

VAMJ	N. K. Verghese and D. Allstot, "Verification of RF and Mixed-Signed Integrated Circuits for Substrate Coupling Effects", in <i>Proc. of IEEE Custom Integrated Circuits Conf.</i> , 1997, pp. 363-370
VAMJ	M. Xu, D. Su, D. Shaeffer, T. Lee, and B. Wooley, "Measuring and Modeling the Effects of Substrate Noise on LNA for a CMOS GPS Receiver", <i>IEEE Journal of Solid-State Circuits</i> , vol. 36, pp. 473-485, 2001.
VAMJ	R. Gharpurey, "A Methodology for Measurement and Characterization of Substrate Noise in High Frequency Circuits," in <i>Proc. of IEEE Custom Integrated Circuits Conf.</i> , 1999, pp. 487-490.
VAMJ	M. Nagata, J. Nagai, K. Hijikata, T. Morie, and A. Iwata, "Physical Design Guides for Substrate Noise Reduction in CMOS Digital Circuits", <i>IEEE Journal of Solid-State Circuits</i> , vol. 36, pp. 539-549, 2001.
VAMJ	M.-D. Ker, T.-Y. Chen, C.-Y. Wu, and H.-H. Chang, "ESD Protection Design on Analog Pin With Very Low Input Capacitance for High-Frequency or Current-Mode Applications", <i>IEEE Journal of Solid-State Circuits</i> , vol. 35, pp. 1194-1199, 2000.
VAMJ	M.-D. Ker, "Whole-Chip ESD Protection Design with Efficient VDD-to-VSS ESD Clamp Circuit for Submicron CMOS VLSI", <i>IEEE Trans. on Electron Devices</i> , vol. 46, pp. 173-183, 1999

Examiner	Victor A. Mandalaga	Date Considered	12-13-02
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INFORMATION DISCLOSURE CITATION

Atty. Docket No. 065120.0070-00	Serial No. 10/062,714
Applicant Ming-Dou KER, et al.	
Filing Date February 5, 2002	Group: 2811

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Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
VAMJ	6,081,002	06/27/2000	Amerasekera et al			
VAMJ	5,754,381	05/19/1998	Ker			
VAMJ	5,465,189	11/07/1995	Polgreen et al.			
VAMJ	5,225,702	07/06/1993	Chatterjee			
VAMJ	5,012,317	04/30/1991	Rountre			
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

VAMJ	C. Richier, P. Salome, G. Mabboux, I. Zaza, A. Juge, and P. Mortini, "Investigation on Different ESD Protection Strategies Devoted to 3.3V RF Applications (2 GHz) in a 0.18 μ m CMOS Process," in <i>Proc. of EOS/ESD Symp.</i> , 200, pp. 251-259.
VAMJ	T.-Y. Chen and M.-D. Ker, "Design on ESD Protection Circuit With Low and Constant Input Capacitance," in <i>Proc. of IEEE Int. Symp. on Quality Electronic Design</i> , 2001, pp. 247-247.
VAMJ	M.-D. Ker, T.-Y. Chen, C.-Y. Wu, and H.-H. Chang, "ESD Protection Design on Analog Pin With Very Low Input Capacitance for RF or Current-Mode Applications," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 35, pp. 1194-1199, 2000.

Examiner Victor A. Mandalaga	Date Considered 12-13-02
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INFORMATION DISCLOSURE CITATION

Atty. Docket No.	067200070-00	Serial No.	10/062,714
Applicant	Ming-Dou KER, et al.		
Filing Date	February 5, 2002	Group:	2811

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Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
VAMS	5,629,544	05/13/97	Voldman et al.			
VAMS	6,034,397	03/07/00	Voldman			
VAMS	5,940,258	08/17/99	Duvvury			
VAMS	5,807,791	09/15/98	Bertin et al			
VAMS	5,719,737	02/17/98	Maloney			
VAMS	5,654,862	08/05/97	Worley et al.			

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

VAMS	S.Voldman, et al., "Semiconductor Process and Structural Optimization of Shallow Trench Isolation-Defined and Polysilicon- Bound Source/Drain Diodes for ESD Networks," in Proc. of EOS/ESD Symp., 1998, pp. 151-160
VAMS	S. Voldman, et al., "Analysis of Snubber-Clamped Diode-String Mixed Voltage Interface ESD Protection Network for Advanced Microprocessors," in Proc. of EOS/ESD symposium, 1995, pp. 43-61.
VAMS	M.J. Pelgrom, et al., "A 3/5 V Compatible I/O Buffer," IEEE Journal of Solid-State Circuits, vol.30, no. 7, pp.823-825, July 1995.
VAMS	G.P. Singh, et al., "High-Voltage-Tolerant I/O Buffers with Low-Voltage CMOS Process," IEEE Journal of Solid-State Circuits, vol.34, no. 11, pp. 1512-1525, Nov. 1999.
VAMS	H. Sanchez, et al., "A Versatile 3.3/2.5/1.8-V CMOS I/O Driver Built in 02. - μ m, 3.5-nm Tox, 1.8 -V CMOS Technology," IEEE Journal of Solid-State Circuits, vol.34 no. 11.pp. 1501-1511, Nov. 1999

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